Amendments to the Specification:

Please replace paragraph [0004] at page 2, line 15 to page 3, line 9 with the following amended paragraph:

[0004] FIG. 1A through FIG. 1F depict a sequence of steps to form a typical trenched DMOS device. In FIG. 1A, an N-type epitaxial layer 10 is formed on an N+ silicon substrate 1. A thermal oxidation process is then performed to grow an initial oxide layer 20 over a location of a termination structure. By using the initial oxide layer 20 as a mask, P-type dopants are implanted to form a P-type active area 12 in the epitaxial layer 10. In FIG. 1B, a plurality of DMOS trenches 13 extending from the P-type active area 12 to the epitaxial layer 10 below the P-type active area 12 is formed by etching. Afterward, an oxidation process is performed to form a gate oxide layer 21 over the P-type active area 12 and to make the initial oxide layer 20 become a field oxide layer 22. In FIG. 1C, a polysilicon layer is deposited by a chemical vapor depositing (CVD) process. The portion of the polysilicon layer on the surface of the epi layer 10 and outside the DMOS trenches is removed by etching, so that a plurality of poly gates 30 is formed respectively in the DMOS trenches 13. Afterward, as shown in FIG. 1D, a lithographic process is carried out to define a location of source regions 40 and to form a photoresist layer 40PR as a mask. N-type dopants are implanted into the active area 12 to form N+ source regions 40 surrounding the DMOS trenches 13. In FIG. 1E, an isolation layer 50 is formed. An etching process is performed to form a plurality of contact windows 51 of the active area over the N+ source regions 40. P-type dopants are implanted to form P+ regions 41 surrounding the N+ source regions 40. As shown in FIG. 1F, a metal contact layer 60 of the source regions is then deposited over the isolation layer 50. The metal contact layer 60 contacts the P-type active area 12 through the contact windows 51. The metal contact layer 60 has an opening over the field oxide layer 22 to expose the isolation layer 50. In addition, a metal contact layer 61 of drain regions [[61]] is formed on the backside of the N+ silicon substrate 1. A driving voltage can be applied to the metal contact layer 61 and 60, while a control voltage is applied to the polysilicon gate 30 to decide whether the source region and drain region of the DMOS are conductive with each other.

Please replace paragraph [0009] with the following amended paragraph:

[0009] In order to solve the above problem, there have been some designs proposed. FIG. 2, depicts a conventional DMOS device and its termination structure, as described in U.S. Patent No. 6,309,929. The '929 patent uses an epitaxial layer to form an active area 12 of the DMOS device and also uses a first trench 14 as the main portion of the termination structure. Afterward, a gate oxide layer 21 and a polysilicon layer are subsequently formed (not shown). The polysilicon re-fills the first trench 14 and a plurality of DMOS trenches 13. Without a lithographic process, the redundant polysilicon layer is removed by an etchback in order to form a plurality of polysilicon gates 30 and a polysilicon sidewall 33 of the first trench 14. Afterward, the exposed gate oxide layer 21 is removed, and then a dielectric oxide layer 53 is deposited. Without a lithographic process, the redundant dielectric oxide layer 53 is removed by an etchback process in order to make the dielectric oxide layer cover the surface of the polysilicon gates 30 and the polysilicon sidewall 33. Thereafter, a TEOS layer 54 is deposited and then processed by the lithographic and etching processes to define the source regions 40. Afterward, a source metal layer 60 is deposited. Through a lithographic and etching process, the source metal layer 60 only covers the [[body region]] P-type active area 12 and extends toward the termination structure by a certain distance.